Claims

[c1] 1. A buried bit line formed in a substrate of a semiconductor device, comprising a shallow doped region, disposed in the substrate;
a deep doped region, disposed in the substrate under a part of the shallow doped region, wherein the shallow doped region and the deep doped region together serve as a buried bit line of the memory device;

[c2] 2. The buried bit line of claim 1, wherein forming the shallow doped region and the deep doped region comprises:forming a patterned mask layer on a substrate;performing a first doping in the substrate not covered by the mask layer to form the shallow doped region, using the mask layer as a mask;forming a liner layer with a predetermined thickness on at least a side surface of the mask layer; andperforming a second doping in the substrate not covered by the mask layer and the liner layer to form a deep doped region, using the liner layer and the mask layer as a mask.

[c3] 3. The buried bit line of claim 2, wherein the mask layer comprises a photoresist material, polysilicon or a dielectric material.

[c4] 4. The buried bit line of claim 2, wherein the liner layer comprises a high molecular weight material layer formed by plasma enhanced chemical vapor deposition.

[c5] 5. The buried bit line of claim 2, wherein an implantation energy for forming the deep doped region is about 50 KeV to 120 KeV and an implantation energy for forming the shallow doped region is about 40 KeV to 80 KeV.

[c6] 6. The buried bit line of claim 1, wherein dopant concentrations in the deep doped region and the shallow doped region are about the same.

[c7] 7. The buried bit line of claim 1, wherein a dopant concentration in the shallow doped region is about 10^{21} /cm ^{3} to 10^{22} /cm3

[c8] 8. The method of claim 5, wherein a dopant concentration in the deep doped region is about 10^{21} /cm ^{3} to 10^{22} /cm ^{3}.

[c9] 9. A fabrication method for a buried bit line, comprising:
forming a patterned mask layer on a substrate;
forming a shallow doped region in the substrate not covered by the mask layer;
forming a liner layer with a predetermined thickness on at least a side surface of the mask layer; and
forming a deep doped region in the substrate not covered by the liner layer and the mask layer, wherein the shallow doped region and the deep doped region together serve as a buried bit line.

[c10] 10. The method of claim 9, wherein the mask layer is formed with a photoresist material, polysilicon or a dielectric material.

[c11] 11. The method of claim 9, wherein the liner layer is formed with a high molecular weight material.

[c12] 12. The method of claim 11, wherein liner layer is reworked directly when deviations occur in a critical dimension after the liner layer is formed.

[c13] 13. The method of claim 9, wherein the liner layer is formed by plasma enhanced chemical vapor deposition.

[c14] 14. The method of claim 9, wherein the deep doped region is formed with an implantation energy of about 50 KeV to 120 KeV..

[c15] 15. The method of claim 9, wherein the shallow doped region is formed with an implantation energy of about 40 KeV to 80 KeV.

[c16] 16. The method of claim 9, wherein dopant concentrations in the deep doped region and in the shallow doped region are about the same.

[c17] 17. A memory device, comprising:
a substrate;
a gate, disposed on a part of the substrate;
a gate oxide layer, disposed between the substrate and the gate;
a shallow doped region, disposed in the substrate beside both sides of the gate; and
a deep doped region, disposed in the substrate under a part of the shallow

doped region, wherein the shallow doped region and the deep doped region together serve as a buried bit line of the memory device.

[c18] 18. The memory device of claim 17, wherein forming the shallow doped region and the deep doped region further comprises:
forming a patterned mask layer on the substrate;
performing a first doped region in the substrate not covered by the mask layer to form the shallow doped region;
forming a liner layer with predetermined thickness on at least a side surface of the mask layer; and
performing a second doped region in the substrate not covered by the liner layer and the mask layer to form a deep doped region.

[c19] 19. The method of claim 18, wherein the mask layer is formed with a photoresist material, polysilicon, or a dielectric material.

[c20] 20. The method of claim 18, wherein the liner layer comprises a high molecular weight material layer formed by plasma enhanced chemical vapor deposition.

[c21] 21. The method of claim 18, wherein the deep doped region is formed with an implantation energy of about 50 KeV to 120 KeV and the shallow doped region is formed with an implantation energy of about 40 KeV to 80 KeV.

[c22] 22. The method of claim 17, wherein dopant concentrations in the deep doped region and in the shallow doped region are about the same.

[c23] 23. The method of claim 17, wherein a dopant concentration in the deep doped region is about 10^{21} /cm ^{3} to 10^{22} /cm3

[c24] 24. The method of claim 17, wherein a dopant concentration in the shallow doped region is about 10^{21} /cm ^{3} to 10^{22} /cm ^{3}.